**Lab Report: 3**



**Digital System Design Lab**

**Spring 2023**

**Submitted by:**

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**Semester: 6**

“On my honor, as a student of University of Engineering and Technology Peshawar, I have neither nor received unauthorized assistance on this academic work”

**Submitted to:**

**Eng:Muhammad Usman**

**LAB 3 Implementation of Gates in Xilinx**

# Objectives

Objectives of this lab are to get familiar with

* How to implement gates in XILINIX
* Observe the result on FPGA

# FPGA

FPGAs are programmable digital logic circuits. It can be programmed to do almost any digital function. There are at least 5 companies making FPGAs in the world. Xilinx is the biggest name in the FPGA world.

The FPGA kits available in our labs are SPARTAN-6 STARTER KIT BOARD.

# XILINX

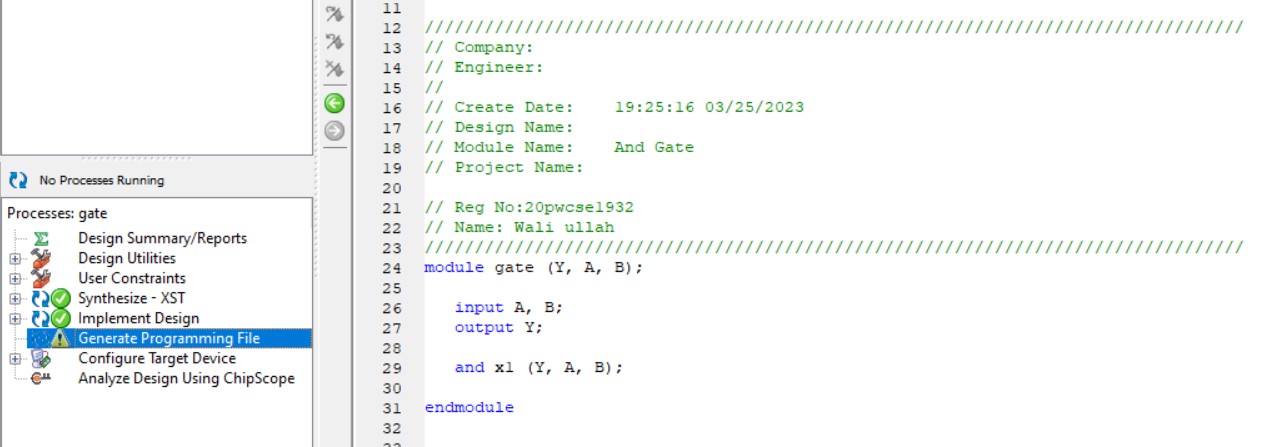
The Integrated Software Environment (ISE™) is the Xilinx® design software suite that allows us to take our design from design entry through Xilinx device programming.

# Steps

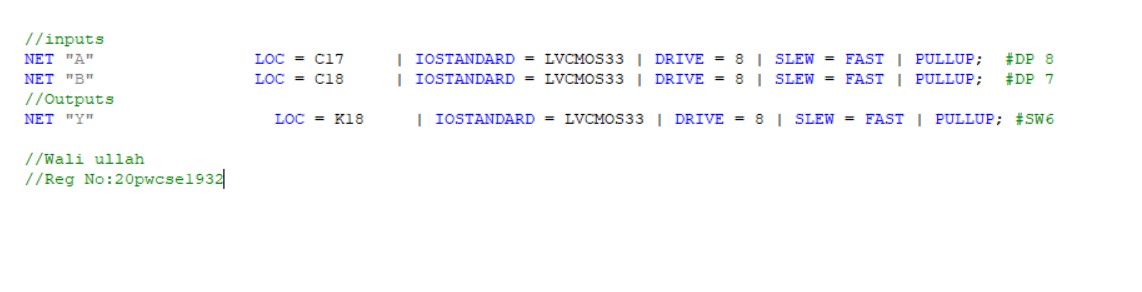
We perform following task by using following steps:

1. First of all the USER DEFINED CONSTRAINT file is created and added in the Project
2. Code is then synthesized.
3. Design is implemented.
4. Programming file is then generated which can be downloaded into the FPGA.

## Task 01 Verilog Code And gate

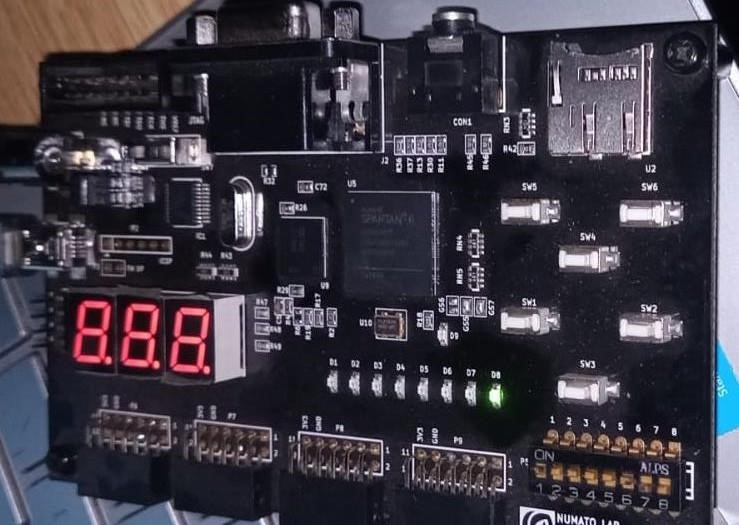


## Design Implementation

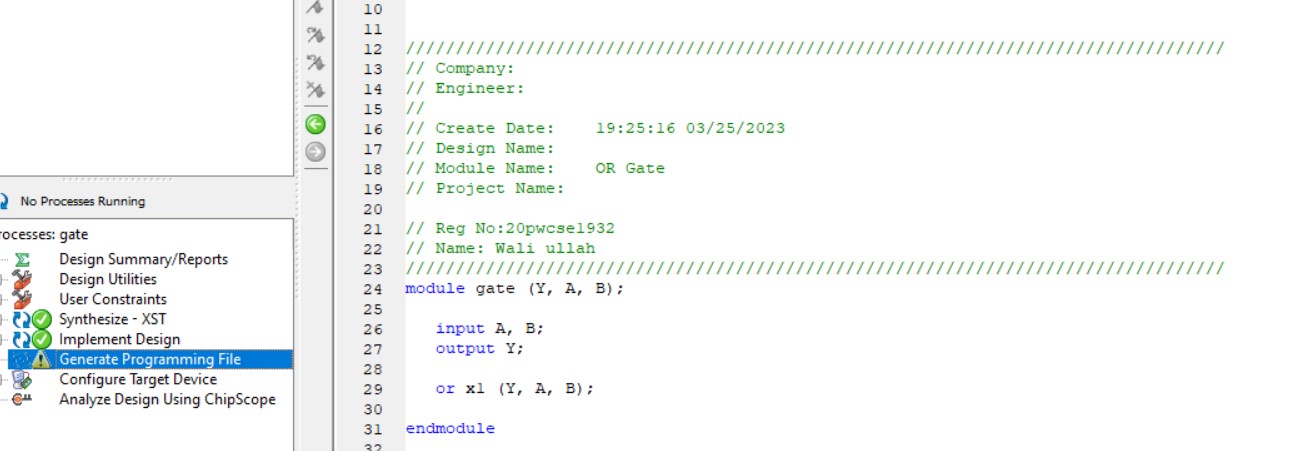


## Output

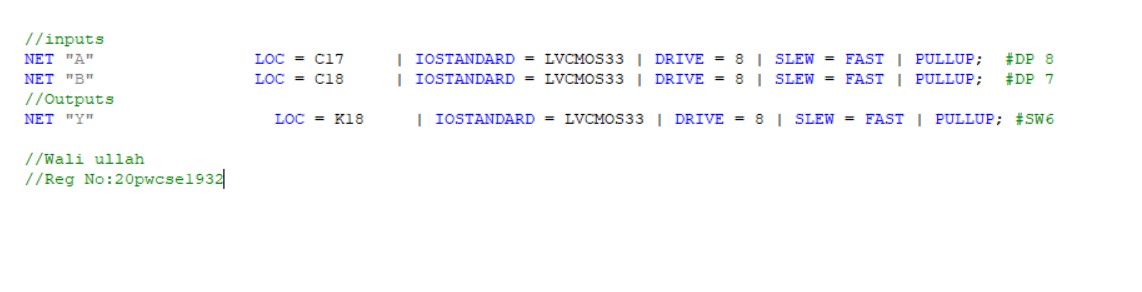
When A=1 , B=1 Then the output Y= 1, which is shown as follows:



## Task 02 Verilog Code OR gate

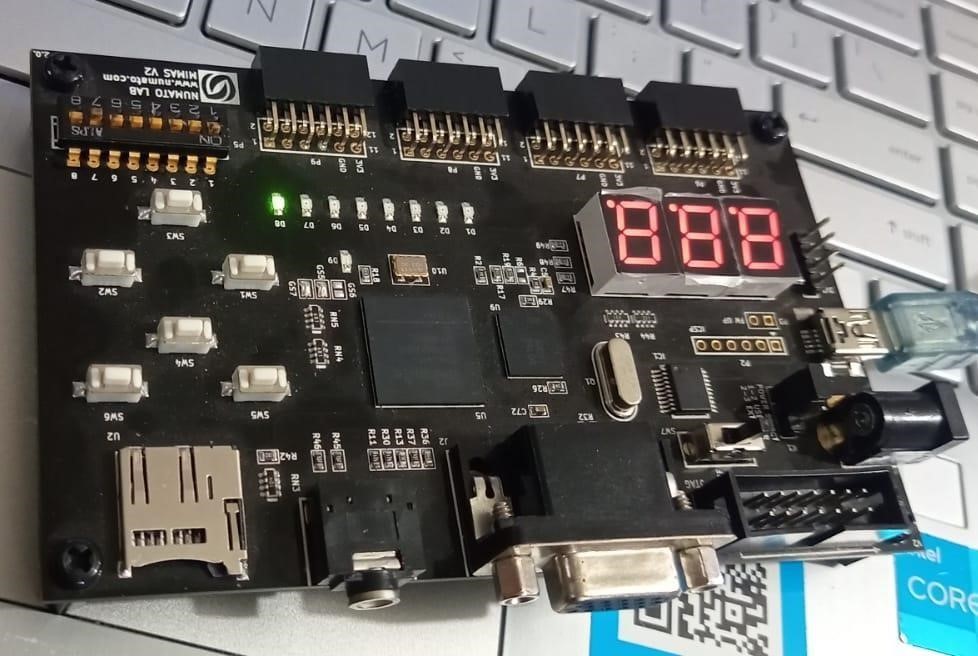


## Design Implementation

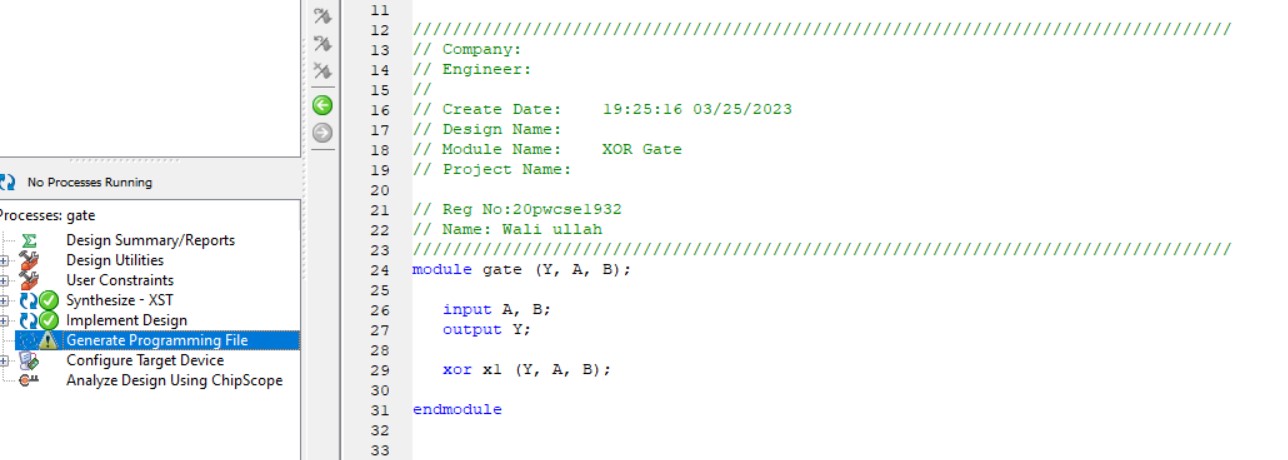


## Output

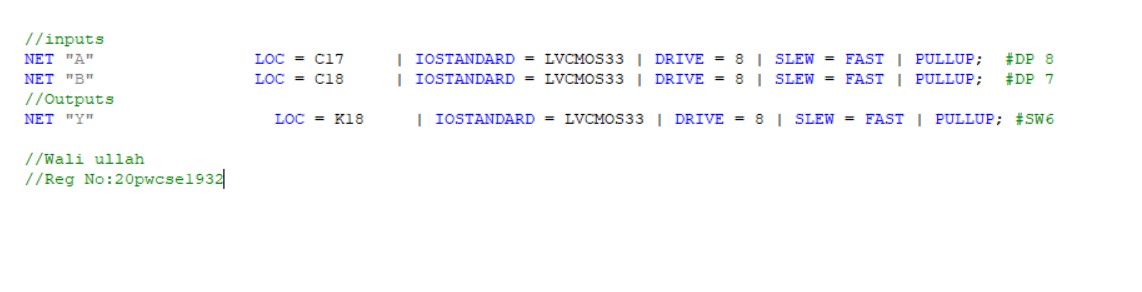
When A=0, and B=1, then output Y=1 which is shown as follows:



## Task 03 XOR Gate Verilog Code

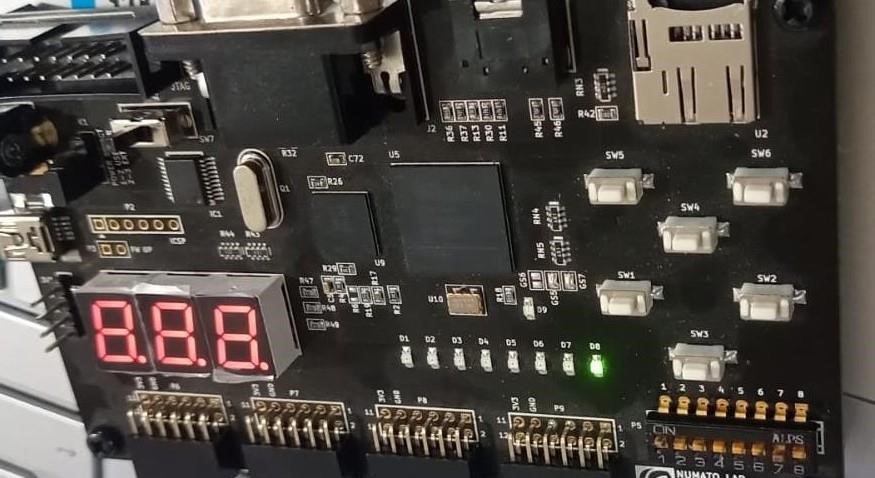


## Design Implementation

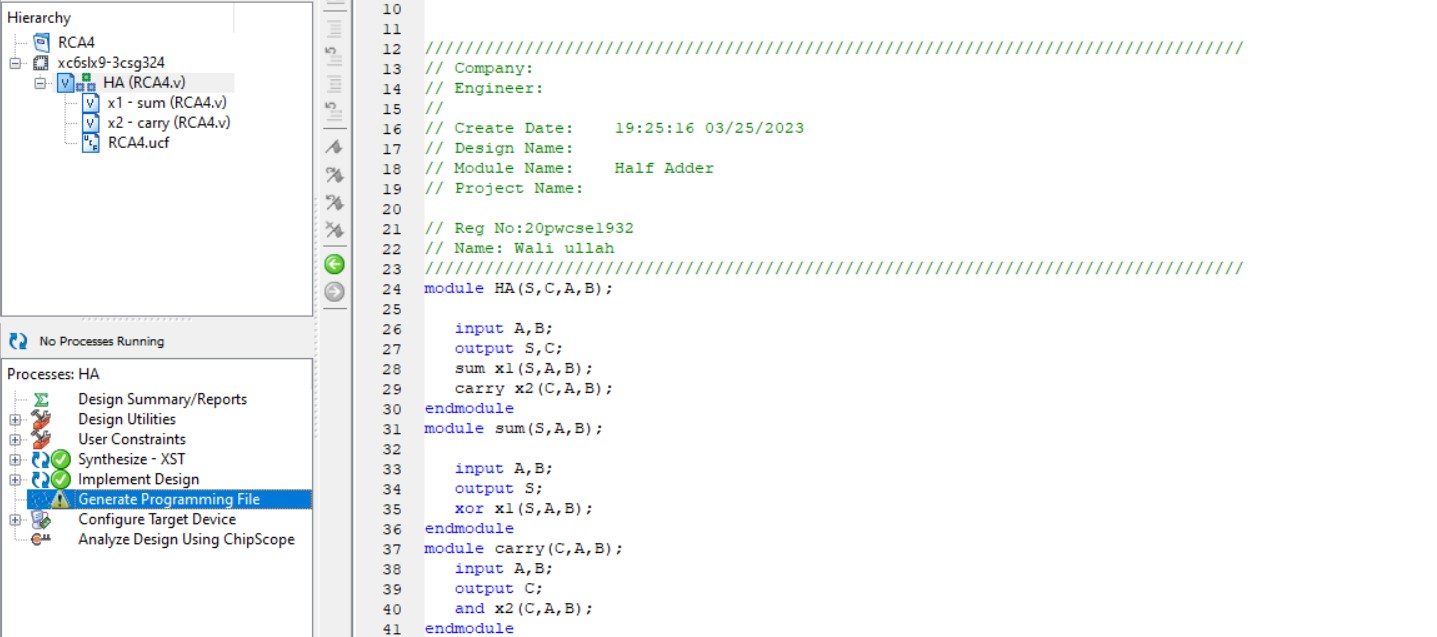


## Output

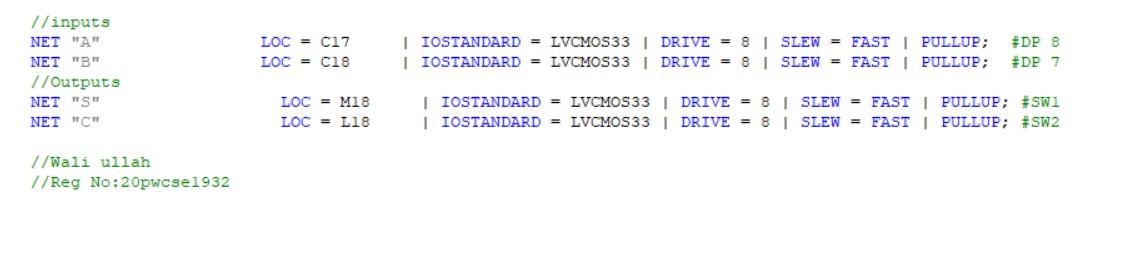
When A=1 and B=0 then the Y=1 which is hsown as follows:



## Task 04 Half Adder Verilog Code

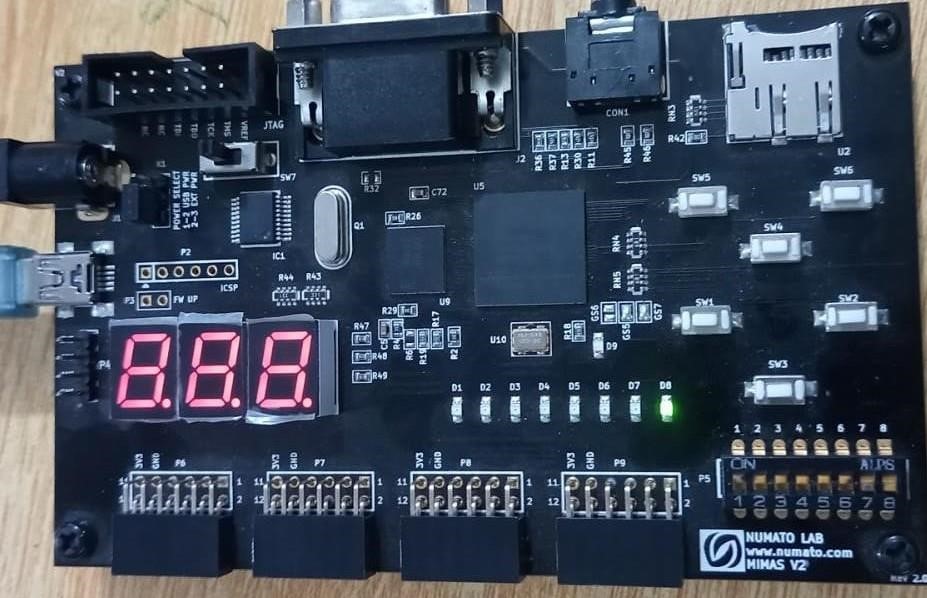


## Design Implementation

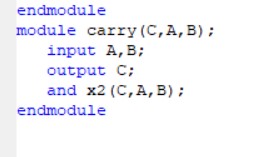
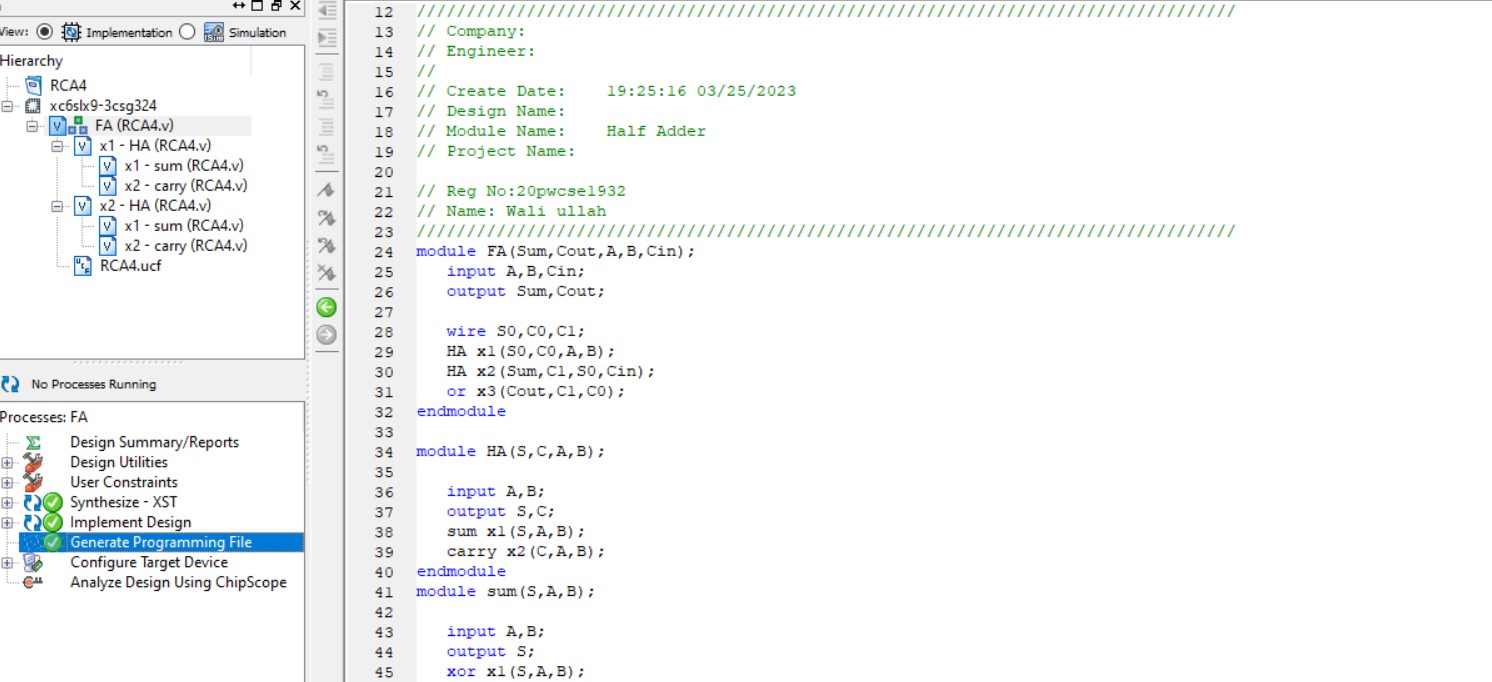


## Output

When A=1 and B=1 then the carry= 1 and sum=0 which is shown as follows:



## Task 05 Full Adder Verilog Code



## Design Implementation

